REMARKS

Claims 22-24 are pending in this application. By this Amendment, claims 22 and 24 are amended. No new matter is added by this Amendment. Support for the language added to claims 22 and 24 is found at, for example, pages 27, line 5 to page 29, line 5 of the specification and Fig. 4.

I. Rejection Under 35 U.S.C. §103(a)

Claims 22-24 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 5,977,997 (Vainsencher) in view of U.S. Patent No. 6,301,430 (Oguro). This rejection is respectfully traversed.

Claims 22 and 24 recite first and second frame buffers each of which stores decoded data for one frame by the decoder, a RAM which stores the decoded data read out from one of the first and second frame buffers, a driver or driving section which is connected to an electrode of the display section, and a controller which controls a decode timing of the decoder, a read timing from the RAM and the driver or driving section, wherein the controller causes the decoded data to be written into one of the first and second frame buffers from which decoded data is not output to the RAM.

Thus, according to the presently claimed invention, the RAM stores decoded data as display data, and the display section or the decoder reads out the decoded data from the RAM and drives the display section. Furthermore, the first and second frame buffers each of which stores display data for one frame are provided, and the controller causes the decoded data to be written into one of the first and second framed buffers from which decoded data is not output to the RAM. Accordingly, the decoded data from the decoder is read out from one of the first and second frame buffers and written into the RAM in a manner that the write speed of the display data for one frame is faster than the read speed of the display data for one frame.

Vainsencher and/or Orguro fail to teach or suggest these features or the benefits associated therewith. More specifically, Vainsencher and/or Orguro fail to teach or suggest 1) including first and second frame buffers each of which stores decoded data for one frame, 2) controlling the write speed of the decoded data from one of the first and second frame buffers to be written into RAM to be faster than the read speed of the display data to be read out from the RAM; and 3) writing the decoded data into one of the first and second frame buffers from which the decoded data is not output to the RAM, and at the same controlling the writing of the decoded data into the RAM in a manner described above.

As discussed above, Vainsencher and Oguro fail to teach or suggest expanding the decoded compressed data (which is supplied as a bitstream) in the frame buffer and subsequently writing the decoded data into the RAM while controlling the write speed of the decoded data. Therefore, even if Vainsencher and Oguro are combined, data which has been written into the RAM is overwritten by data in the next frame and the quality of a displayed image ends up being degraded. In particular, when compressed data is continuously supplied as a bitstream, it is extremely difficult to control driving of the display section.

However, in the presently claimed invention, even when compressed data is continuously supplied as a bitstream, data written into the RAM is never overwritten, and it is possible to prevent the quality of displayed images from being degraded by employing simple control.

For the foregoing reasons claims 22 and 24, and claim 23 depending therefrom are not rendered obvious by Vainsencher and/or Oguro.

Withdrawal of the rejection is requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the pending claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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